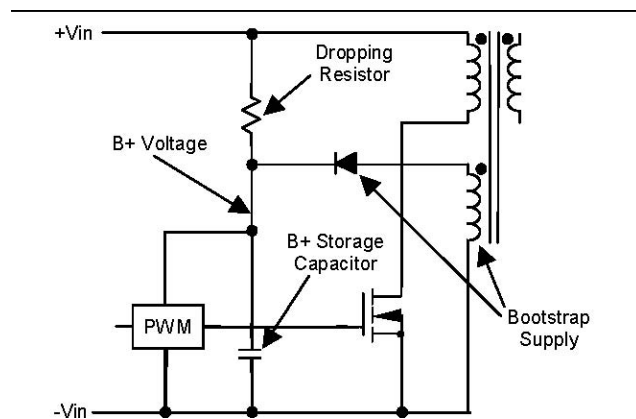


## Non-Redundant Paralleling of $\mu$ V300 Modules

### General Description

When paralleling  $\mu$ V300 Series modules for more power and without redundancy, simply connecting the parallel pins together will result in slow system startup times. The circuit presented here allows the  $\mu$ V300 Series modules to startup quickly without using the PDMs.



### Background

The 300V series of MicroVerter modules uses a bootstrap supply and a dropping resistor in order to generate the required B+ voltage to run the PWM circuit (see Figure 11a). When power is first applied, all of the capacitors in the module are discharged and there is no B+ voltage to run the PWM. A large resistor connected from the input voltage to the B+ voltage provides a trickle current to slowly charge the B+ capacitors. The PWM circuit remains off until the B+ voltage reaches a level that is safe for operation. It then turns on and begins providing power to both itself and the load. If the PAR pin is held low, the module is disabled and can't produce any power. The PWM circuits must then operate from the energy stored in the B+ capacitors. Eventually, that energy runs out and the PWM must shut down.

During the time that the PWM circuits are off, the PAR pin is held low by the control IC. In the case where the Parallel pins of two or more modules are directly connected together, the

PWM of one module will hold the parallel pin of the other modules in the off state. Only when all of the modules try to start simultaneously will the system start. This can take several seconds with two modules up to several minutes with four or more modules.

### Implementation

The circuit shown in Figure 11b solves the startup problem of the  $\mu$ V300 series by disconnecting the PAR pins of the modules until all of the modules are active. Once all of the modules are active, their PAR pins are connected together and the modules share the load current. The operation of the circuit is as follows:

Initially, all of the modules are off and un-powered. When power is first applied, all of the PAR pins are in a low impedance state to the -IN of the modules. The PAR pin's IV characteristics are similar to a forward biased diode with a  $V_f$  of 0.6V to 1.4V. The current drawn by the PAR pins shuts off Q3 via the common anode diodes, D1x. Resistors R9x from each PAR pin to the -IN pin minimize the circuit's sensitivity to variations in the " $V_f$ " of the PAR pins. While Q3 is held off, Q2 turns on and disables the series FET switches, Q1x, by pulling their gates low. Q2 turning on also lowers the base voltage of Q4 via resistor R8. Q4 is an active clamp that limits the voltage of the share bus to 1.4V. Each module's PAR pin is connected to the share bus via the body diode of the corresponding series FET switch. This limits the PAR pin voltages to about 2V above the -IN pin. This voltage is high enough to allow the modules to start (the modules shut down at ~1V) but not high enough to bring up the output of the module (Note: the modules output current is roughly proportional to the PAR pin voltage over 1V. Because the PAR pin voltage is limited, the module can't produce enough current to drive the load).

Now that the module has started, it can generate its own power from the input voltage via its bootstrap supply. Q4 and the body diodes of the Q1x series switches keep the modules in this idle state until all of the modules have started allowing Q3 to turn on. This turns off Q2, and R2 pulls the gates of the series switches high – connecting the PAR pins together and enabling current sharing. R2 and R8 raise the base voltage of Q4 to about 4.1V. This moves the clamping level of the active clamp above the

operational voltage range of the PAR pins, effectively removing the clamp. The base of Q4 is limited to 4.1V so that the base-circuit. Since the active clamp is now off, the modules can emitter junction will not avalanche if the share bus is pulled all start up in unison, with each one providing an equal low - either by the modules or an additional logic on-off share of the load.

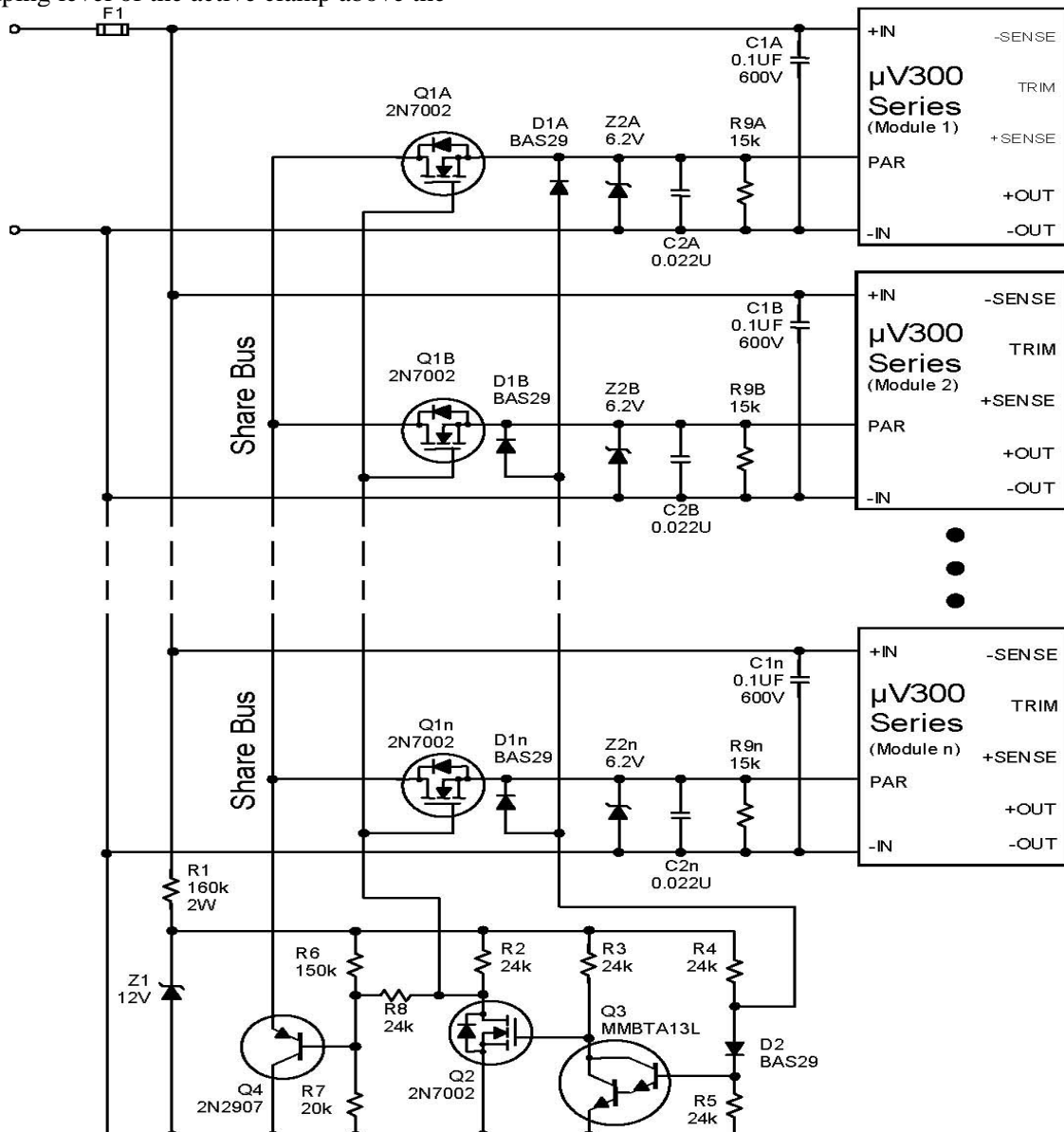


Figure 11b Startup disconnect circuit for non-redundant paralleling of the  $\mu$ V300 series module  
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